13. (Twice Amended) The decoder of Claim 12, wherein the selector comprises a multiplexer, the multiplexer enabling one of the first memory cell group and the second memory cell group in response to the group-select signal.

REMARKS

Responding to paragraphs 1 and 2 of the Office Action, the rejection of claims 6-10 and 12-16 under 35 U.S.C. 112, first paragraph is respectfully traversed.

Regarding subparagraph (a), elements 608a-b are described at page 27, line 5 of the specification. The paragraph beginning on page 26, line 24 has been amended to include a description of element 640. Element 640 is labeled GSA. A GSA is shown in FIG. 3 as element 302 and is described at page 23, lines 11-12 as a global sense amplifier. As a result, no new matter has been added.

Regarding subparagraph (b), the paragraph beginning at page 32, line 17 has been amended to include a description of elements M1-M7, M10-M12, M16 and I13. M8 and M14 are described as PMOS devices at page 32, line 29 and page 33, line 6, respectively. From this description and the drawing, a person skilled in the art would be able to identify the other PMOS transistors shown in FIG. 8. NMOS transistors 1140 and 1141 are shown in FIG. 11 and are described at page 35, lines 30-31. A person skilled in the art would be able to identify the other NMOS transistors shown in FIG. 8 from the description of NMOS transistors 1140 and 1141. No new matter has been added. Elements I12 and I13 in FIG. 8 use the standard symbol for an inverter and have been described as such in the amendment to the specification. No new matter has been added.

Regarding subparagraph (c), FIG. 11 is described on pages 35 and 36 of the specification, although the figure number is not included in the description.

Regarding subparagraph (d), the paragraph beginning on page 36, line 13 has been amended to include a description of the predecoder and gwd shown in FIG. 12. A predecoder and gwd are described in FIG. 6, page 26, lines 29-32. Similar language has been added to the amended paragraph. No new matter has been added.

Regarding subparagraph (e), the paragraph beginning at page 39, line 32 has been amended to include a description of the elements identified by the Examiner. The inputs and outputs are identified by the direction of the arrows in FIG. 17 in which the elements appear. No new matter has been added.

Regarding subparagraphs (f) – (h), the subject matter of the Figures identified by the Examiner are not needed to describe the invention claimed in this application. As stated in Amendment A, embodiments of the claimed invention are shown in FIGS. 8, 12, 16 and 17. Subparagraphs (f) – (h) address FIGS. 19, 21 and 22B.

Regarding subparagraph (i), column redundancy embodiments are shown in FIGS. 14, 15A and 15B. FIG. 14 illustrates a column redundancy fuse system embodiment. Page 39, lines 17-24 state that in the embodiment of FIG. 16, selector device 1620 may be a fuse system, and that selector 1600 may implement column redundancy. The foregoing is a teaching to a person skilled in the art that the selector 1600 of the FIGS. 16-17 embodiment can be used as a column redundancy selector. Those skilled in the art would know how to combine the teachings of FIGS. 14, 15A, 15B, 16 and 17 and related specification text to provide a column redundancy selector of the type claimed in claims 9 and 15.

Responding to paragraphs 3 and 4 of the Office Action, the rejection of claims 6, 9 and 12-13 under 35 U.S.C. 112, second paragraph, is respectfully traversed.

Claim 6 has been amended to overcome the rejection by providing that the decoder decodes an address to enable the second memory cell group. This amendment is supported by the embodiment described at page 26, line 29 to page 27, line 2.

Regarding claim 9, the reasons for overcoming the rejection were explained in response to subparagraph (i) above.

Claim 12 has been amended in a manner analogous to claim 6 and the rejection has been overcome for the same reasons explained in connection with claim 6.

Claim 13 has been amended to provide that the multiplexer enables one of the first memory cell group and the second memory cell group. It is believed that this amendment puts the claim in compliance with § 112.

Responding to paragraphs 5-6 of the Office Action, the rejection of claims 1-2 and 4 under 35 U.S.C. 102(b) as being anticipated by Tomita (U.S. Patent No. 5,886,941) is respectfully traversed. Regarding the asynchronous portion, Tomita states at Col. 14, lines 51-59:

> The series of operations in the first embodiment are constructed such that the address decoder is actuated at the rising edge of the clock signal CK, executed in asynchronous manner up to completion of the cycle, and is not affected by variation of the delay time of the input drive signals in each decoding circuit, and also the decoding operation starts

immediately after determination of the input drive signal. For this reason, a high-speed operation can be effected.

Regarding the synchronous portion, Tomita describes the operation of the address driver in relation to the CK clock signal at Col. 1, lines 51-64:

> FIG. 21 is a circuit diagram, which shows a structural example of the address driver 1002. Driving circuits D.sub.0 through D.sub.7 provided to respectively correspond to address signals A.sub.0 to A.sub.7 all have the same circuit structure. In the drive circuit D.sub.n corresponding to the address signal A.sub.n, a D-type flip-flop circuit (F/F circuit) 200 latches the address signal A.sub.n at a rising edge of a clock signal CK. Output of the F/F circuit 200 is outputted as the drive signal d.sub.n via NOT circuits 201, 202, and is further outputted as the drive signal rd.sub.n via a NOT circuit 203. Namely, the drive signal d.sub.n outputs a logical level of the same phase as that of the address signal A.sub.n and the drive signal rd.sub.n outputs a logical level whose phase is opposite to that of the logical level of the address signal A.sub.n.

Claim 1 as amended is limited to:

c. a feedback-resetting portion comprising an input <u>receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal</u>, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

Nothing in Tomita teaches or suggests this novel feedback-resetting portion. The Examiner relies on reset signal R from the output of NAND gate 105 shown in FIG. 4. FIG. 4 illustrates details of the control circuit 1 shown in FIG. 1. Assuming for purposes of argument that the decoding circuits of Tomita correspond to the asynchronous portion of claim 1 and the address driver 2 of Tomita correspond to the synchronous portion of claim 1 as the Examiner apparently contends, control circuit 1 does not receive an input signal from the decoding circuits. At best, control circuit 1 sends an output signal EN to the decoding circuits. Control circuit also does not transmit an output signal to address driver 2 in response to the input signal as claimed. Control circuit 1 transmits a signal NPR to address driver 2, but the NPR signal is not transmitted in response to any signal received from the decoding circuit. The NPR signal is generated in response to the SEL signal and the CLK signal (Col. 8, lines 40-42), not any signal received from the decoding circuits.

The feedback arrangement relied on by the Examiner within the control circuit is local to the control circuit and results in a mode of operation divorced from the operation achieved by the claimed feedback-resetting portion that transmits an output signal to the synchronous portion in response to an input signal received from the asynchronous portion. For all these reasons, amended claim 1 is allowable.

Claims 2 and 4 are dependent on claim 1 and are allowable for the same reasons as claim 1.

Responding to paragraphs 7-8 of the Office Action, the rejection of claims 6-10 and 12-16 under 35 U.S.C. 103(a) as being unpatentable over Akizawa et al. (U.S. Patent No. 5,398,206) ("Akizawa") in view of Tomita is respectfully traversed.

The amendment to claim 6 is supported by the embodiments described on page 36, lines 27-34:

> Although it may be simpler to provide redundant memory cell circuits that can be activated during product testing during the manufacturing stage, it may also be desirable to activate selected redundant memory cells when the memory product is in service, e.g., during maintenance or on-the-fly during product operation. Such activation can be effected by numerous techniques and support circuitry that are well known in the art.

Amended claim 6 is limited to:

> d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable the second memory cell group responsive to a group-select signal.

Nothing in Akizawa or Tomita, taken singly or in combination, teaches or suggests such a selector. The Examiner states that Akizawa describes a word line selection detecting circuit 200 being controlled by group select signals 205 and 206 (page 5 of the Office Action). However, as explained at Col. 5, lines 28-34, circuit 200 is a detecting circuit that detects only portions of memory with defects that are identified in the manufacturing process (emphasis supplied):

> Accordingly, if the semiconductor memory device is a mask ROM, for example, the compensated area is determined in accordance with data when the data is written into the memory array 300 in the course of

manufacturing process of the memory device. The specific word lines to which the circuit 200 should be electrically connected are determined in accordance with an arrangement of the compensated area for the data to be written in the memory array 300.

Nothing in Akizawa or Tomita teaches or suggests a decoder that decodes an address to enable a second memory cell group responsive to a group-select signal in the event of a fault detected on a first memory output when the decoder is in service. As pointed in the above quote from page 36 of the specification, the subject matter of claim 6 overcomes the limitations of prior art decoders, such as those described by Akizawa, by providing for operation when the memory product is in service, e.g., on-the-fly. Thus, Akizawa or Tomita, taken singly or in combination, could not achieve the operation resulting from the claimed decoder. For all the foregoing reasons, claim 6 is allowable.

Claims 7-10 are dependent on claim 6 and are allowable for the same reasons as claim 6.

Claim 12 has been amended in a manner analogous to claim 1 and claim 6 and is allowable for the same reasons as claims 1 and 6.

Claims 13-16 are dependent on claim 12 and are allowable for the same reasons as claim 12.

In summary, each of claims 1-2, 4, 6-10 and 12-16 is allowable, and such action is respectfully requested.

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Respectfully submitted,

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Version of Amended Specification and Claims
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In The Specification:

Kindly delete the paragraph beginning "FIG. 6" at page 26, line 24 and ending "or both" at page 27, line 12, and replace it with the following paragraph:

FIG. 6 illustrates a hierarchical structure 600 having hierarchical word-line decoding in which each hierarchical memory module 605 is composed of a predefined number of memory cells 610, which are coupled with a particular local word line decoder 615a-c. Each local word line decoder 615a-c is coupled with a respective global word line decoder 620. Each global word line decoder 620a-d is activated when predecoder 622 transmits address information relevant to a particular global word line decoder 620a-d via predecoder lines 623. In response, global word line decoder 620a-d activates global word line 630 which, in turn, activates a particular local word line decoder 615a-c. Local word line decoder 615a-c then enables associated memory module 605, so that the particular memory cell 610 of interest can be evaluated. Each of memory modules 605 can be considered to be an independent memory component to the extent that the hierarchical functionality of each of modules 605 relies upon local sensing via local sense amplifiers 608a-b, local decoding via local word line decoders 615a-c, or both. Global sense amplifiers (GSA), such as GSA 640, also are shown. As with other preferred embodiments of the invention herein, it is desirable to have each module 605 be self-timed. Self-timing can be especially useful when used in conjunction with local word line decoding because a local timing signal from a

respective one of memory module 605 can be used to terminate global word line activation, local bitline sensing, or both.

Kindly delete the paragraph beginning "FIG. 8" at page 32, line 17 and ending "buffer delay" at page 32, line 25, and replace it with the following paragraph:

FIG. 8 is a circuit diagram illustrative of an asynchronously-resettable decoder 800 according to this aspect of the present invention. FIG. 8 illustrates PMOS transistors M5, M6, M7, M8, M10, M11, M12, M13 and M14, and NMOS transistors M0, M1, M2, M3, M4 and M16. Inverters I12 and I13 also are connected as shown. It may be desirable to implement the AND function, for example, by source-coupled logic. The capacitance on the input x2_n 802 can be generally large, therefore the AND function is performed with about one inverter delay plus three buffer stages. The buffers are skewed, which decreases the load capacitance by about one-half and decreases the buffer delay.

Kindly delete the paragraph beginning "In FIG. 12," at page 36, line 13 and ending "in the art" at page 36, line 34, and replace it with the following paragraph:

In FIG. 12, memory structure 1200, composed of hierarchical functional memory modules 1201 is preferred to have at least one or more redundant memory rows 1202, 1204; one, or more redundant memory columns 1206, 1208; or both, within each module 1201. It is preferred that the redundant memory rows 1202, 1204, and/or columns 1206, 1208 be paired, because it has been observed that bit cell failures tend to occur in pairs. Module-level redundancy, as shown in FIG. 12, where redundancy is implemented using a preselected number of redundant memory rows 1202, 1204, or redundant memory columns 1206, 1208, within memory module 1201, can be a very

area-efficient approach provided the typical number of bit cell failures per module remains small. By implementing only a single row 1202 or a single column 1206 or both in memory module 1201, only one additional multiplexer is needed for the respective row or column. As explained in connection with FIG. 6, each global word line decoder (GWD) is activated when a predecoder transmits address information relevant to a particular GWD via precoder lines. Although it may be simpler to provide redundant memory cell circuits that can be activated during product testing during the manufacturing stage, it may also be desirable to activate selected redundant memory cells when the memory product is in service, e.g., during maintenance or on-the-fly during product operation. Such activation can be effected by numerous techniques and support circuitry which are well-known in the art.

Kindly delete the paragraph beginning "FIG. 17" at page 39, line 32 and ending "and 1702" at page 40, line 15, and replace it with the following paragraph:

FIG. 17 illustrates a preferred embodiment of selector 1600 in FIG. 16, in the form of decoder 1700 with row redundancy as realized in a hierarchical memory environment. Decoder 1700 may be particularly suitable for implementing module-level redundancy, such as that described relative to module 1200 in FIG. 12. Global decoder 1700, can operate similarly to the manner of asynchronously-resettable decoder 800 of FIG. 8. As shown in FIG. 17, decoder 1700 includes inputs shift, shift_n_Prev, xL_Prev, x1, x2_n, x2_n_Prev, shutInH (1703), shift_n, and outputs xL_Next, shutoutH, and WL. In general, decoder 1700 can be coupled with a first, designated memory row, and a second, alternative memory row. Although the second row may be a physical row adjacent the first memory row, and another of the originally designated rows of the

memory module, the second row also may be a redundant row which is implemented in the module. Although row decoder 1700 decodes the first memory row under normal operations, it also is disposed to select and decode the second memory row in [responsive] response to an alternative-row-select signal. Where the second row is a redundant row, it may be more suitable to deem the selection signal to be a "redundant-row-select" signal. The aforementioned row select signals are illustrated as inputs 1701 and 1702.

In The Claims:

Kindly amend claims 1, 6, 12 and 13 as follows:

1. (Twice Amended) An address decoder for a memory cell, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a line for the memory cell; and

c. a feedback-resetting portion [, coupled with] comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, [and the asynchronous portion and interposed there between,] the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

6. (Twice Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable [the first memory cell group, and being disposed to select and decode] the second memory cell group responsive to a group-select signal.

12. (Twice Amended) A decoder in a memory module having a plurality of memory cell groups, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a selected memory cell group;

c. a feedback-resetting portion [, coupled with] comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, [and the asynchronous portion and interposed there between,] the feedback-resetting portion substantially isolating the

synchronous portion from the asynchronous portion responsive to an asynchronous reset signal;

d. a signal input;

e. a first memory output coupled with a first memory cell group;

f. a second memory output coupled with a second memory cell group; and

g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable [the first memory cell group, and being disposed to select and decode] the second memory cell group responsive to a group-select signal.

13. (Twice Amended) The decoder of Claim 12, wherein the selector comprises a multiplexer, the multiplexer [selecting to decode from] enabling one of the first memory cell group and the second memory cell group [, the multiplexer being responsive] in response to the group-select signal.